IN THE CLAIMS

Please amend the claims as follows:

1-10. (Cancelled)

11. (Currently Amended) A clock receiver circuit device comprising:

a first input adapted to be connected with a first connection of a semi-conductor component to receive a first clock signal;

a second input adapted to be connected with a second connection of the semi-conductor component to receive a second clock signal inversely equal to the first clock signal; and

~~wherein the~~ a receiver circuit ~~device comprises~~ comprising more than three transfer gates, the receiver circuit converting the first clock signal and the second clock signal into respective inversely equal clock output signals having voltage levels different from voltage levels associated with the received first and second clock signals.

12. (Original) The receiver circuit device according to claim 11, which comprises four transfer gates.

13. (Original) The receiver circuit device according to claim 11, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

14. (Original) The receiver circuit device according to claim 13, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input,

inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

15. (Original) The receiver circuit device according to claim 14, comprising wherein at a second transfer gate connected with the first transfer gate, a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

16. (Original) The receiver circuit device according to claim 11, comprising wherein at a third transfer gate a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

17. (Original) The receiver circuit device according to claim 16, comprising wherein at a fourth transfer gate connected with third transfer gate, a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with first input of the receiver circuit device.

18. (Original) The receiver circuit device according to claim 11, in which differential clock signals are present at the first and second inputs.

19. (Currently Amended) A clock receiver circuit device comprising:

a first input adapted to be connected with a first connection of a semi-conductor component to receive a first clock signal;

a second input adapted to be connected with a second connection of the semi-conductor component to receive a second clock signal inversely equal to the first clock signal; ~~and~~

~~wherein the~~ a receiver circuit ~~device comprises more than three transfer gates, wherein a signal detectable between a first and second transfer gate and/or a second signal detectable between a third and fourth transfer gate, is used to boost a clock relaying circuit~~ converting the first clock signal and the second clock signal into respective inversely equal clock output signals having voltage levels different from voltage levels associated with the received first and second clock signals;

a first transfer gate and a third transfer gate, each of the first transfer gate and the third transfer gate having a corresponding first transfer gate control connection ~~is~~ connected with the second clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, connected with the first clock input of the clock receiver circuit device; and

a second transfer gate and a fourth transfer gate, each of the second transfer gate and the fourth transfer gate having a corresponding first transfer gate control connection ~~is~~ connected with the first clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, connected with the second clock input of the clock receiver circuit device, wherein corresponding further connections of the transfer gates are connected to apply a first voltage to a further connection of both the first transfer gate and the fourth transfer gate, and a second voltage, different from the first voltage, to a further connection of both the second transfer gate and the third transfer gate.

Claims 20-23. (Canceled)

24. (Currently Amended) A clock receiver circuit device comprising:

a first clock input for receiving a first clock signal;

a second clock input for receiving a second clock signal, inversely equal to the first clock signal;

wherein at a first transfer gate a corresponding first transfer gate control connection is connected with the second clock input of the clock receiver circuit device, and a corresponding

second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the first clock input of the clock receiver circuit device; and

wherein at a second transfer gate a corresponding first transfer gate control connection is connected with the first clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the second clock input of the clock receiver circuit device,

wherein corresponding further connections of the transfer gates are connected with each other and are jointly connected with a clock output for emitting a clock output signal having a voltage level different from voltage levels associated with the received first and second clock signals.

25. (Currently Amended) A semi-conductor component having a receiver comprising:

a clock receiver circuit device comprising:

a first input adapted to be connected with a first connection of a semi-conductor component to receive a first clock signal;

a second input adapted to be connected with a second connection of the semi-conductor component to receive a second clock signal inversely equal to the first clock signal; and

~~wherein the~~ a receiver circuit device comprises more than three transfer gates, the receiver circuit device converting the first clock signal and the second clock signal into respective clock output signals having voltage levels different from voltage levels associated with the received first and second clock signals.

26. (Original) The component according to claim 25, wherein the receiver device circuit comprises four transfer gates.

27. (Original) The component according to claim 25, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation

to the first transfer gate control input, is connected with the first input of the receiver circuit device.

28. (Original) The component according to claim 27, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

29. (Original) The component according to claim 28, comprising wherein at a second transfer gate connected with the first transfer gate, a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device;

wherein at a third transfer gate a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device; and

wherein at a fourth transfer gate connected with third transfer gate, a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with first input of the receiver circuit device.

30. (Currently Amended) A clock receiver circuit device comprising:

a first clock input for receiving a first clock signal;

a second clock input for receiving a second clock signal, inversely equal to the first clock signal;

~~wherein at~~ a first transfer gate and a third transfer gate, each of the first transfer gate and the third transfer gate having a corresponding first transfer gate control connection ~~is~~ connected

with the second clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, connected with the first clock input of the clock receiver circuit device; and

~~wherein at~~ a second transfer gate and a fourth transfer gate, each of the second transfer gate and the fourth transfer gate having a corresponding first transfer gate control connection ~~is~~ connected with the first clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, connected with the second clock input of the clock receiver circuit device, wherein corresponding further connections of the transfer gates are connected ~~with each other and are jointly connected with a clock output for emitting a clock output signal~~ to apply a first voltage to a further connection of both the first transfer gate and the fourth transfer gate, and a second voltage, different from the first voltage, to a further connection of both the second transfer gate and the third transfer gate.

31. (Currently Amended) A clock receiver circuit device comprising:

means for a first input adapted to be connected with a first connection of a semi-conductor component to receive a first clock signal;

means for a second input adapted to be connected with a second connection of the semi-conductor component to receive a second clock signal inversely equal to the first clock signal; and

means for converting the first clock signal and the second clock signal into respective inversely equal clock output signals having voltage levels different from voltage levels associated with the received first and second clock signals, wherein the receiver circuit device comprises more than three transfer gates.